

REMARKS

Applicants hereby add new claims 29-36. Accordingly, claims 1-13 and 15-36 are pending in the present application.

Claims 1, 3-13, 15-17, 19-22, and 27 stand rejected under 35 USC 102(b) for anticipation by U.S. Patent No. 4,794,441 to Sugawara. Claim 2 and 14 stand rejected under 35 USC 103(a) for obviousness by U.S. Patent No. 4,175,240 to Kremlev. Claim 18 stands rejected under 35 USC 103(a) for obviousness over Sugawara. Claims 23-26, and 28 stand rejected under 35 USC 103(a) for obviousness over Sugawara and further in view of U.S. Patent No. 6,023,155 to Kalinsky.

Applicants respectfully traverse the rejections and urge allowance of the present application.

Referring to claim 1, the Office Action states that FETs 11, 12 are coupled in parallel to form a power semiconductor switching device. The Office Action is in error. Sugawara is replete with teachings of circuit constructions comprising a control section and a main drive section. The main drive section conducts current intermediate nodes A, B using an npn transistor 9 in the disclosed embodiments, and control circuitry operates to control npn transistor 9 to conduct the main drive currents.

Referring to the teachings in col. 7 of Sugawara identified in the Office Action, terminals G1 and G2 (corresponding to the gate control terminals of FETs 10, 11) are *control* terminals which operate to control conduction of currents within transistor 9 as set forth in col. 7, lines 34-69. Col. 8, lines 1-10 specify that npn transistor 9 is a transistor of the main drive section and G1 and G2 comprise control terminals. Transistors 10, 11

operate as control devices for operations of main drive transistor 9 and in no fair interpretation are coupled in parallel to form a power semiconductor switching device as defined in claim 1. The focus of Sugawara is controlling a large amount of electrical power (i.e., intermediate nodes A, B) while using a small control signal as set forth in col. 1, lines 12-15. FETs 10, 11 clearly only operate as control devices and fail to disclose or suggest the power semiconductor switching device as claimed. Positively-recited limitations of claim 1 are not shown nor suggested by the prior art and claim 1 is allowable for at least this reason.

The claims which depend from independent claim 1 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

For example, claim 2 recites the field effect transistors comprise planar transistors. Referring to col. 7, lines 25-27 of Sugawara discloses FET 11 clearly comprises a vertical FET. The Examiner's utilization of teachings of Kremlev is improper and contrary to the explicit teachings of Sugawara. The 103 rejection of claim 2 is improper for at least this additional reason.

Further, the reliance upon "known in the art" rationale as set forth in paragraph 4 is also improper and traversed hereby. Referring to MPEP §2143.01 (8th ed.), there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine reference teachings. The mere fact that references *can* be combined or modified does not render the resultant combination obvious *unless the prior art also suggests the desirability of the*

combination. MPEP §2143.01 citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Initially, the combination presented by the Examiner is contrary to the explicit teachings of Sugawara. Accordingly, there is no motivation to combine the reference teachings.

In addition, there is no motivation apart from bald, cursory statements of the Office Action why one would be motivated to combine the reference teachings. The Federal Circuit discussed proper motivation *In re Lee*, 61 USPQ 2d 1430 (Fed. Cir. 2002). The motivation identified in the Office Action is akin to the conclusory statements set forth in *In re Lee* which were found to fail to provide the requisite motivation to support an obviousness rejection. The Court in *In re Lee* stated the factual inquiry whether to combine references must be through and searching. It must be based on objective evidence of record. The Court in *In re Fritch*, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992) stated motivation is provided only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. The *Lee* Court stated that the Examiner's conclusory statements in the *Lee* case do not adequately address the issue of motivation to combine. The Court additionally stated that the factual question of motivation is material to patentability and can not be resolved on subjective belief and unknown authority. The Court also stated that deficiencies of cited references cannot be remedied by general conclusions about what is basic knowledge or common sense. The Court further stated that the determination of patentability must be based on evidence.

In the instant case, the record is entirely devoid of any evidence to support

motivation to combine the teachings apart from the bald conclusory statements of the Examiner which are insufficient for proper motivation as set forth by the Federal Circuit. The Office cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims but must set forth rationale on which it relied. Statements set forth in the present Office Action are akin to the alleged motivation discussed *In re Lee* and accordingly are insufficient to combine the reference teachings. The 103 rejection of claim 2 is improper without the proper motivation and Applicants respectfully request allowance of claim 2 in the next action.

Referring to claim 3, Sugawara fails to disclose or suggest the gate driver amplifier. No teachings of the prior art are identified as allegedly disclosing the claimed gate driver amplifier. Claim 3 is allowable for this additional reason.

Referring to claim 4, Sugawara is devoid of disclosing the power converter controller as defined. The Examiner fails to provide any rationale as to how switch 1 operates as a power converter controller as alleged. Claim 4 is allowable.

Referring to claim 7, Sugawara is devoid of disclosing the zero current switching/timing circuit as defined. The Examiner fails to provide any rationale as to how switch 1 operates as a zero current switching/timing circuit as alleged. Claim 7 is allowable.

Referring to claim 8, Sugawara is devoid of disclosing the load protection circuit as defined. The Examiner fails to provide any rationale as to how switch 1 operates as a load protection circuit as alleged. Claim 8 is allowable.

Referring to claim 9, Sugawara is devoid of disclosing the active snubber circuit as

defined. Claim 9 is allowable.

Referring to claim 26, the prior art fails to disclose or suggest the limitations of claim 26 wherein the *power semiconductor switching device is configured to operably conduct power currents in excess of 1 Ampere*. The transistors 10, 11 of Sugawara operate as control transistors and in no fair interpretation disclose or suggest operable conduction of the claimed power currents in excess of 1 Ampere. Referring to col. 8, lines 8-9 of Sugawara, only conduction of 10 mA currents is described. No teachings are identified in support of the rejection of claim 26. Limitations of claim 26 are not disclosed nor suggested by the prior art and claim 26 is allowable.

Claim 12 includes limitations of previous claim 14 and recites *forming the power field effect transistor comprising a plurality of planar field effect transistors electrically coupled in parallel and configured to operably conduct power currents*. Transistors 10, 11 of Sugawara comprise control transistors. In addition, transistor 11 of Sugawara comprises a vertical FET. Sugawara fails to disclose or suggest the power field effect transistor comprising the plurality of planar field effect transistors electrically coupled in parallel and configured to operably conduct power currents. Page 3 of the Office Action presents teachings of Kremlev in support of the obviousness rejection of claim 14. Any teachings of Kremlev regarding usage of planar FETs as *switching transistors* are irrelevant to claim 12 defining the plurality of planar field effect transistors electrically coupled in parallel and *configured to operably conduct power currents*. Even if the references are combined, the combination fails to disclose or suggest at least the limitations of claim 12 identified above. Numerous positively-recited limitations of claim 12

are not shown nor suggested by the prior art and claim 12 is allowable.

There is no motivation to combine Kremlev with Sugawara in an obviousness rejection. Sugawara specifically defines one of the parallel coupled transistors as comprising a vertical transistor. Any combination of planar transistor teachings of Kremlev is contrary to the explicit teachings of Sugawara. Claim 12 is allowable over the prior art for at least this additional reason.

The claims which depend from independent claim 12 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

In the event that a rejection of the claims is maintained with respect to the prior art, or a new rejection made, Applicants respectfully request identification *in a non-final action* of elements which allegedly correspond to limitations of the claims in accordance with 37 C.F.R. §1.104(c)(2). In particular, 37 C.F.R. §1.104(c)(2) provides that *the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified*. Further, 37 C.F.R. §1.104(c)(2) states that the Examiner must cite the best references at their command. When a reference is complex or shows or describes inventions other than that claimed by Applicants, the particular teachings relied upon must be designated as nearly as practicable. The pertinence of each reference if not apparent must be clearly explained for each rejected claim specified. Applicants respectfully request clarification of the rejections with respect to specific references and specific references teachings therein pursuant to 37 C.F.R. §1.104(c)(2) in a non-final Action if any claims are not found to be allowable.

Applicants submit an Information Disclosure Statement herewith.

Applicant notes that the references listed on the forms PTO-1449 (copies enclosed) submitted with the Information Disclosure Statement on August 12, 2002 have not been initialed by the Examiner. Applicant requests full consideration of such references and intialing thereof on the forms PTO-1449.

Support for the new claims is provided at least at paragraphs 41 and 108 of the originally-filed application. The new claims are allowable over the prior art

Applicants respectfully request allowance of all pending claims in the next Action.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 3/6/03

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